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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,697	09/22/2003	James M. Cleeves	3558P022D2	6036

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EXAMINER	
NGUYEN, TUAN H	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/665,697	CLEEVES, JAMES M.
	Examiner	Art Unit
	Tuan H. Nguyen	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The disclosure is objected to because of the following informalities: On page 1, next to last line, serial number "09/841,727" should be correctly changed to –09/814,727--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 36, 39-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 36, it is unclear as to how could the first, second and third rail-stacks have approximately the same height when the second rail-stack having more layers than that of the first and the third rail-stacks? (Specification, page 14, [0040]-[0041] that discloses that same height only applies for middle rail-stacks, not for lowest and highest rail-stack levels).

In claim 39, last five lines are confusing and indefinite, since it is unclear as to how could the third rail-stack is formed by etching the third conductive layer, and the etched fourth semiconductor layer which is covered by the antifuse layer, without etching the antifuse layer?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 31-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Knall et al.(cited by applicant).

Knall et al., figs. 1-7 and text on col. 2-10 discloses the claimed method for fabricating two memory levels in a memory array including forming a first conductive layer 14, depositing a doped first semiconductor layer 15 over the first conductive layer 14 (fig. 1, col. 3, paragraphs 2, 3, 4); etching the first conductive layer 14 and the first semiconductor layer 15 into a plurality of first parallel, spaced-apart (half) rail-stacks (col. 3, fourth paragraph); filling and planarizing the space between the first rail-stacks with a first insulator (col. 3, lines 45-47, col. 4, second paragraph); forming a first antifuse layer 20 over the planarized first upper surface (col. 3, lines 41-47); depositing

a doped second semiconductor layer 21 over the first antifuse layer 20; forming a second conductive layer 23 over the doped second semiconductor layer 21; depositing a doped third semiconductor layer 24 over the second conductive layer 23; etching the second semiconductor layer 21, second conductive layer 23, and third semiconductor layer 24 into a plurality of second parallel, spaced-apart (full) rail stacks (col. 3, last paragraph); filling and planarizing the space between the second rail-stacks with a second insulator (col. 4, second paragraph); forming a second antifuse layer 26 on the planarized second upper surface (col. 4, third paragraph); depositing a doped fourth semiconductor layer 28, 30 over the second antifuse 26, forming a third conductive layer 31; etching the doped fourth semiconductor layer 28, 30, third conductive layer 31 to form third parallel, spaced-apart rail-stacks (fig. 1); filling the space between the third rail-stacks with a third insulator (coll. 4, second paragraph).

With respect to claim 32, see col. 3, lines 29-33 which discloses the semiconductor material (first, second third and fourth semiconductor layers) such as silicon layer is typically polysilicon.

With respect to claim 33, 34, fig. 3 shown the concentration of N-,P+ of polysilicon layers 47, 52 having opposite conductivity type for forming diode.

With respect to claim 35, see col. 3, lines 40-45, col. 4, third paragraph for the antifuse material formed from a dielectric such as silicon dioxide.

With respect to claim 36, insofar, as understood, is shown in fig. 3 wherein the full (middle) rail-stacks 3, 4, 5 ,6 having the same number of layers therefore having approximately the same height.

With respect to claim 37, see col. 3, third paragraph for the conductive layers' material including silicide.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cleeves et al., and Vyvoda et al. disclose related methods for forming antifuse structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is 571-272-1694. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan H. Nguyen
Primary Examiner
Art Unit 2813